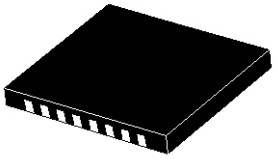
M41T00AUD

Serial real-time clock with audio

Features

- Combination real-time clock with audio
  - Serial RTC based on M41T00
  - Audio section provides:
    - 300mW differential audio amplifier
    - 256 and 512Hz tone generation
    - -33 to +12dB gain, 3dB steps (16 steps plus MUTE)
- Real-time clock details:
  - Superset of M41T00
  - 3.0 to 3.6V operation
    - Timekeeping down to 1.7V
  - Automatic backup switchover circuit
    - Ultra low 400nA backup current at 3.0V (typ)
    - Suitable for battery or capacitor backup
    - On-chip trickle charge circuit for backup capacitor
  - 400kHz I^2C bus
  - M41T00 compatible register set with counters for seconds, minutes, hours, day, date, month, years, and century
    - Automatic leap year compensation
    - HT bit set when clock goes into backup mode
  - RTC operates using 32,768Hz quartz crystal
    - Calibration register provides for adjustments of -63 to +126ppm
    - Oscillator supports crystals with up to 40kΩ series resistance, 12.5pF load capacitance
  - Oscillator fail detect circuit OF bit indicates when oscillator has stopped for four or more cycles



DFN16 (5mm x 4mm)
"D" Suffix

- Audio section
  - Power amplifier
    - Differential output amplifier
    - Provides 300mW into 8Ω (THD+N = 2% (max), f_{in} = 1kHz)
  - Summing node at audio input
    - Inverting configuration with summing resistors into the minus (-) terminal
    - 0dB gain with 10kΩ feedback resistor and 20kΩ input summing resistors
    - Signal input centered at $V_{DD}/2$
    - $1.6V_{P-P}$ analog input range (max)
  - 256 or 512 Hz signal multiplexing with analog input to provide audio with beep tones
  - Volume control, 4-bit register
    - Allows gain adjustment from -33dB to +12dB
    - 3dB steps
    - MUTE bit
  - Audio automatically shuts off in backup mode
- 0°C to 70°C operation
- Small DFN16 package (5mm x 4mm)

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1 Description

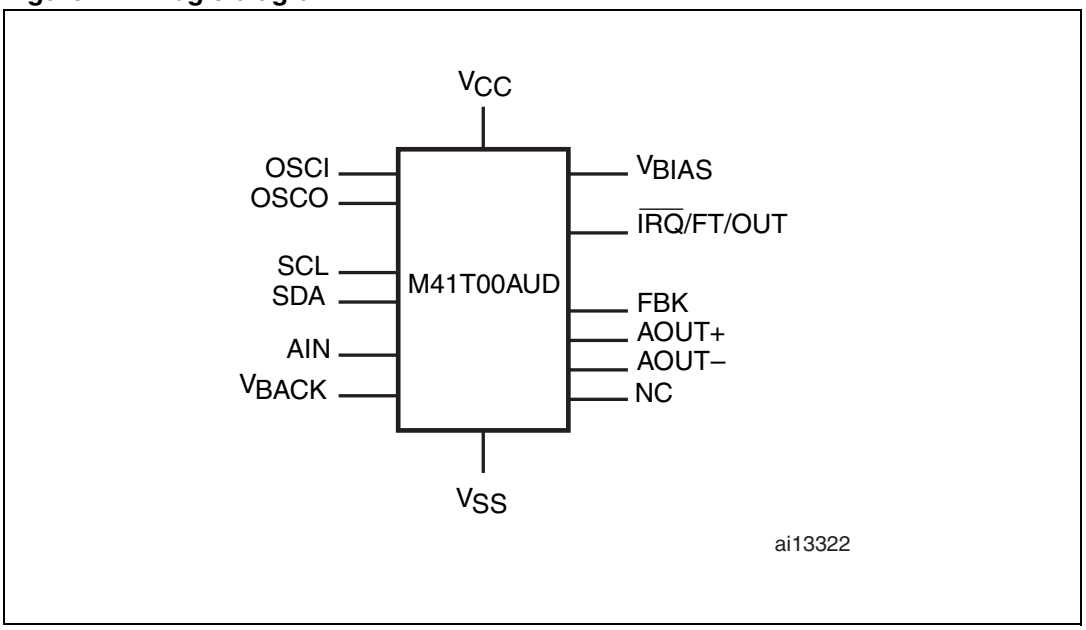
The M41T00AUD is a low power serial real-time clock (RTC) with an integral audio section with tone generator and 300mW output amplifier. The RTC is a superset of the M41T00 with enhancements such as a precision reference for switchover, an oscillator fail detect circuit and storing of the time at power down. The audio section includes a summing amplifier (inverting) at the input. An 8kHz low pass filter follows that with a 16 step programmable gain stage next. A 256 or 512Hz audio tone can be switched into the filter in place of the input signal. From the gain stage, the 300mW amplifier drives the output pins.

The M41T00AUD has a built-in power sense circuit which detects power failures and automatically switches to the backup input when V_{CC} is removed. Backup power can be supplied by a capacitor or by a battery such as a Lithium coin cell. The device includes a trickle charge circuit for charging the capacitor.

The RTC includes a built-in 32.768kHz oscillator controlled by an external crystal. Eight register bytes are used for the clock/calendar functions and are superset compatible with the M41T00. Two additional registers control the audio section and the trickle charger. The 10 registers (see *Table 2*) are accessed over a 400kHz I^2C bus. The address register increments automatically after each byte READ or WRITE operation thus streamlining transfers by eliminating the need to send a new address for each by to be transferred.

Typical data retention times will be in excess of 5 years with a 50mAh 3V lithium cell (see RTC DC characteristics, *Table 12* for more information).

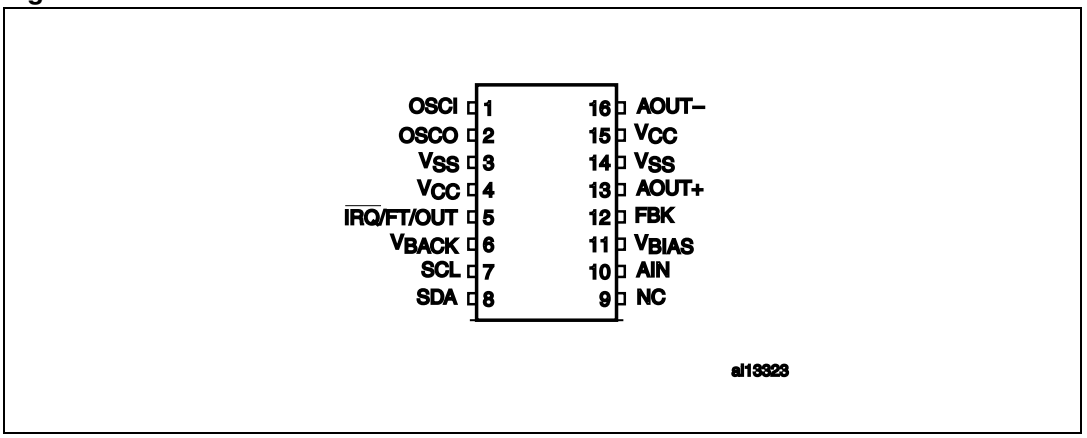
Figure 1. Logic diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection



2.2 Pin description

Table 1. Pin description

Symbol	Name and function
V_{CC}	Supply voltage
OSCI	Oscillator input
OSCO	Oscillator output
SCL	I^2C serial clock
SDA	I^2C serial data
AIN	Audio input
V_{BIAS}	Input for decoupling capacitor
V_{SS}	Ground
AOUT–	Analog out, 180 phase
AOUT+	Analog out, 0 phase
$\overline{IRQ}$/FT/OUT	Interrupt output for oscillator fail detect, frequency test output for calibration, or discrete logic output
V_{BACK}	Backup supply voltage
FBK	Feedback; connect feedback resistor between this pin and AIN
NC	No connection
No name; exposed pad on back of IC package	Must be connected to ground

3 Application

Figure 3. Application diagram

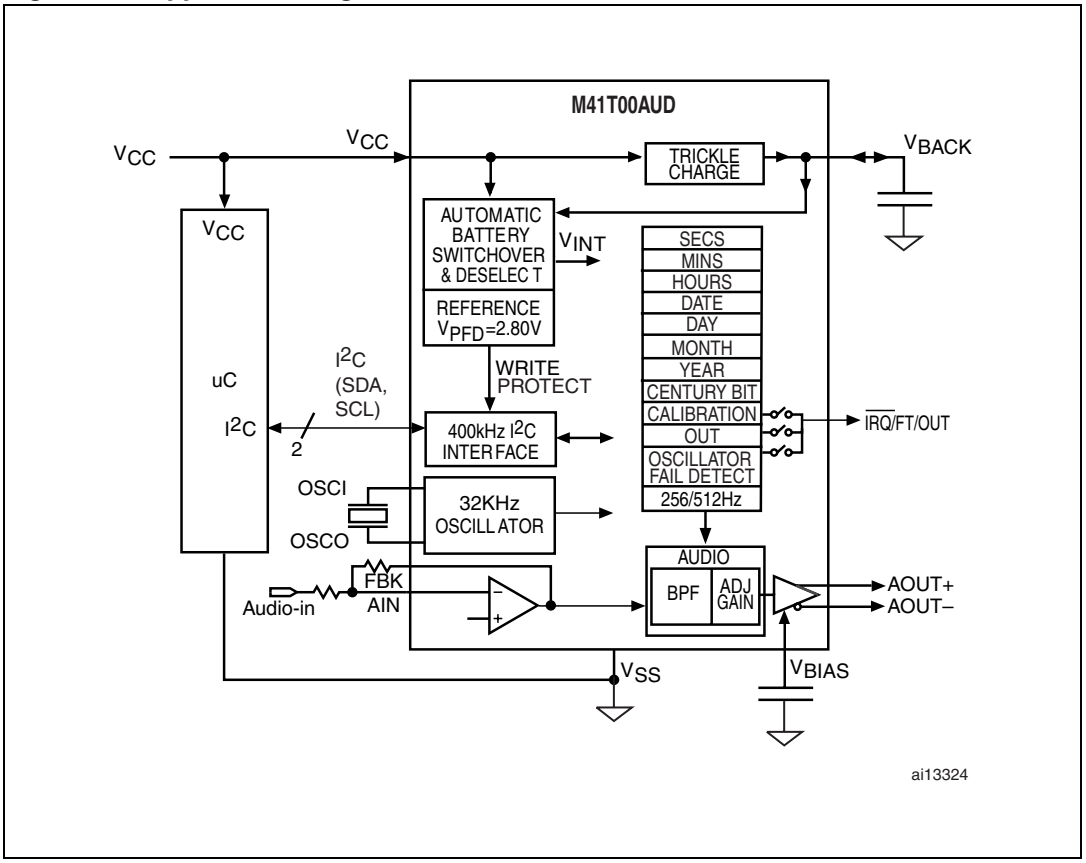
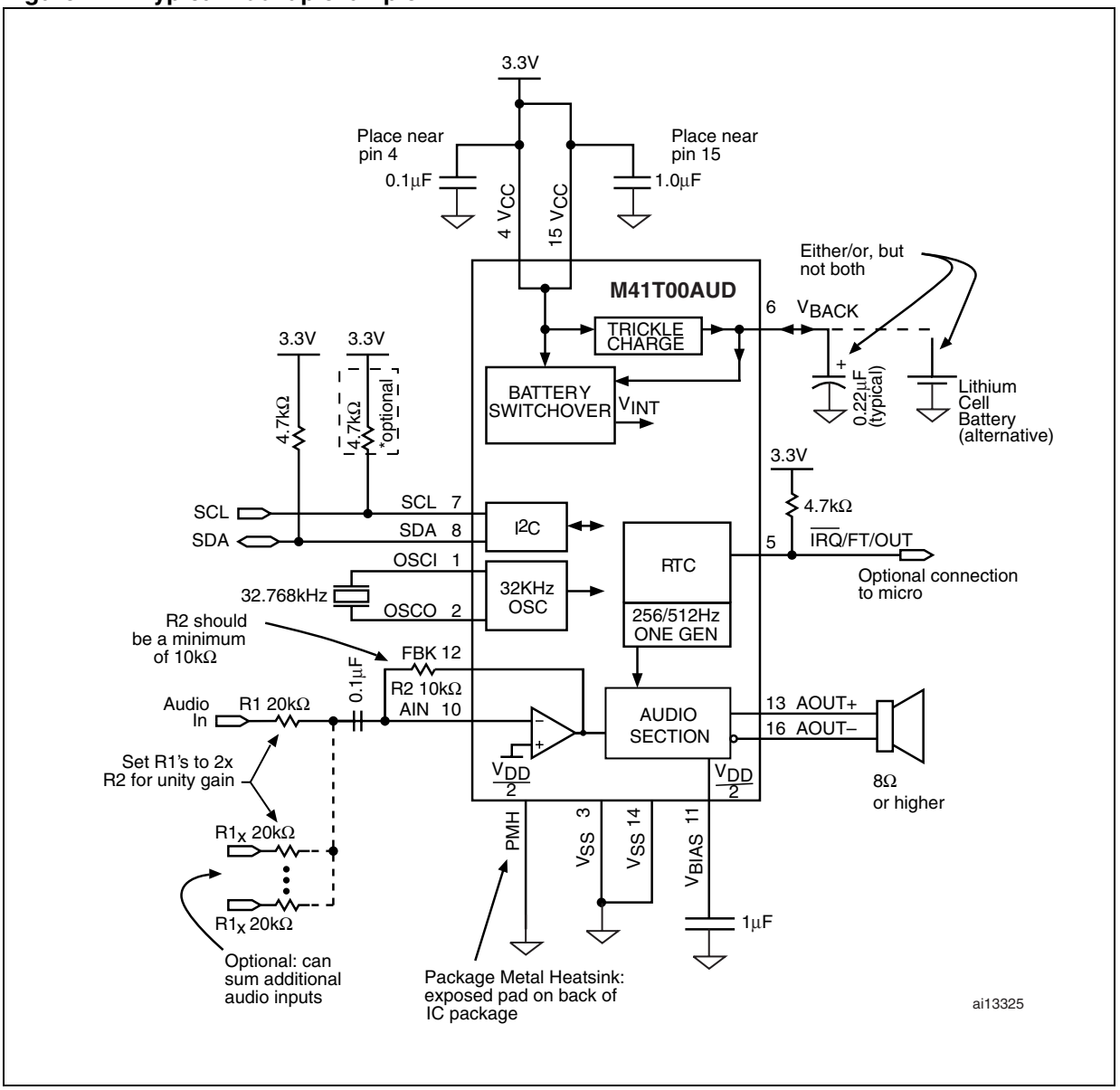


Figure 4. Typical hookup example



4 Operation

The M41T00AUD clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 10 bytes contained in the device can then be accessed sequentially in the following order:

Table 2. List of registers

Byte address	Contents
00h	Seconds register
01h	Minutes register
02h	Century/hours register
03h	Day register
04h	Date register
05h	Month register
06h	Years register
07h	Calibration/control register
08h	Audio register
09h	Control2 register

The M41T00AUD continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the backup battery or capacitor and powers down into an ultra low current mode of operation to conserve battery life. Upon power-up, the device switches from battery to V_{CC} at V_{SO} and recognizes inputs.

4.1 2-wire bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

- Bus not busy. Both data and clock lines remain high.
- Start data transfer. A change in the state of the data line, from high to Low, while the clock is high, defines the START condition.
- Stop data transfer. A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.
- Data valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit. By definition, a device that gives out a message is called "transmitter", the receiving device that gets the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

- Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

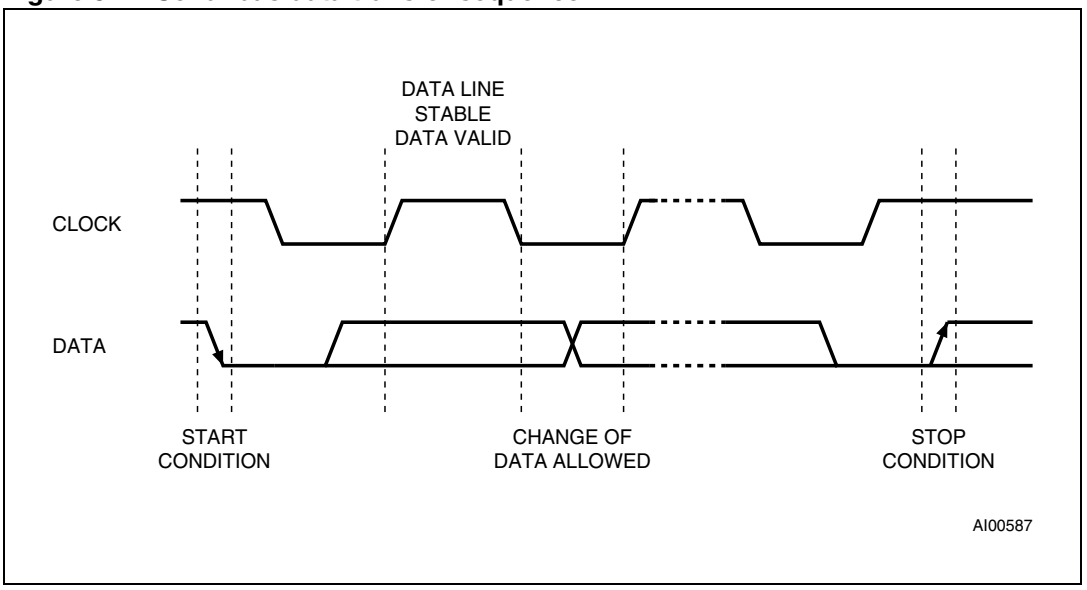


Figure 6. Acknowledgement sequence

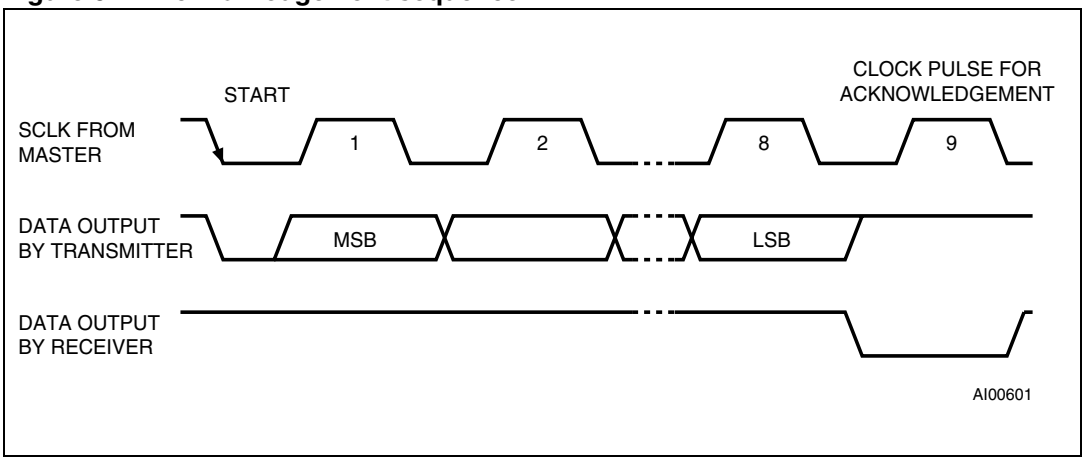
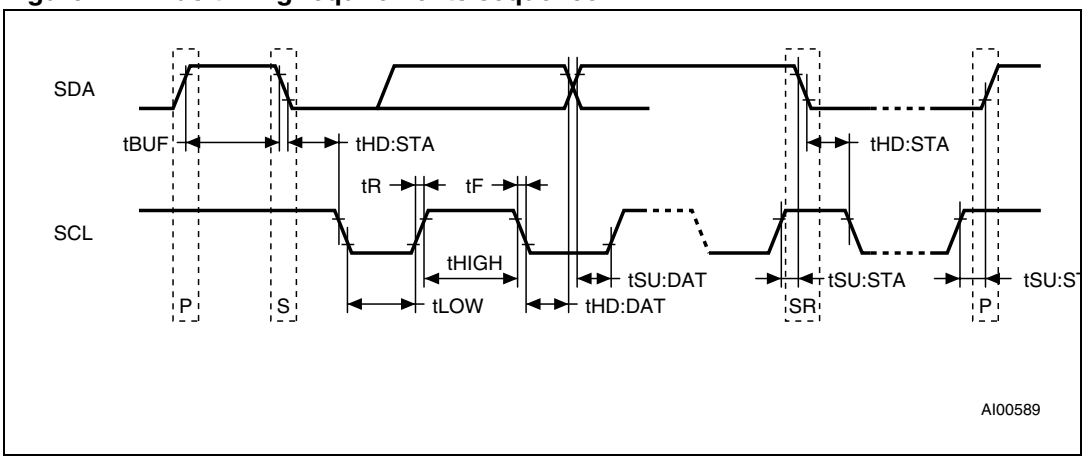


Figure 7. Bus timing requirements sequence



1. P = STOP and S = START

4.2 Characteristics

Table 3. AC characteristics

Symbol	Parameter[1]	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock Low period	1.3			µs
t_{HIGH}	Clock High period	600			ns
t_R	SDA and SCL Rise time			300	ns
t_F	SDA and SCL Fall time			300	ns
$t_{HD:STA}$	START condition Hold time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START condition Setup time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$[2]	Data Setup time	100			ns
$t_{HD:DAT}$	Data Hold time	0			µs
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL.

4.3 READ mode

In this mode, the master reads the M41T00AUD slave after setting the slave address (see *Figure 8*). Following the WRITE mode control bit (R/W = 0) and the acknowledge bit, the word (register) address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The device slave transmitter will now place the data byte at address An+1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented, whereby the master reads the M41T00AUD slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 10*).

Figure 8. Slave address location

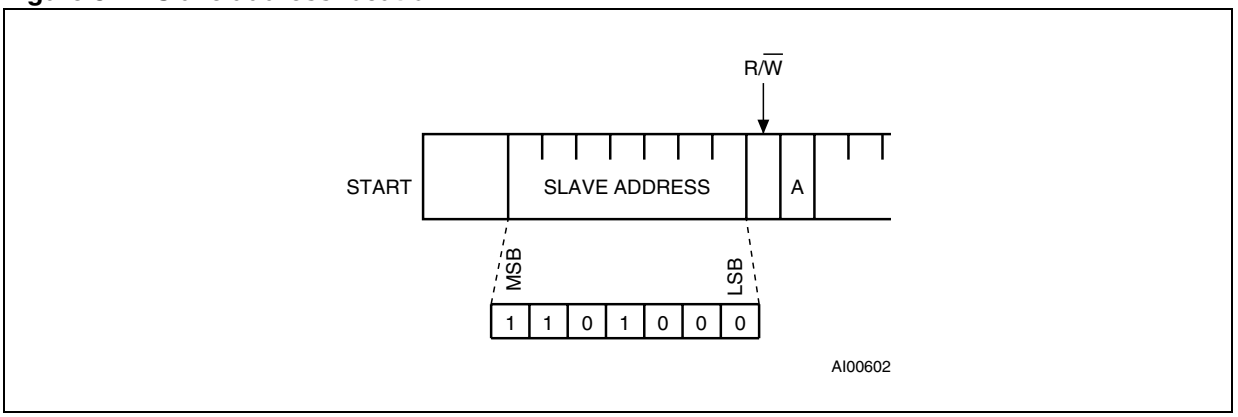


Figure 9. READ mode sequence

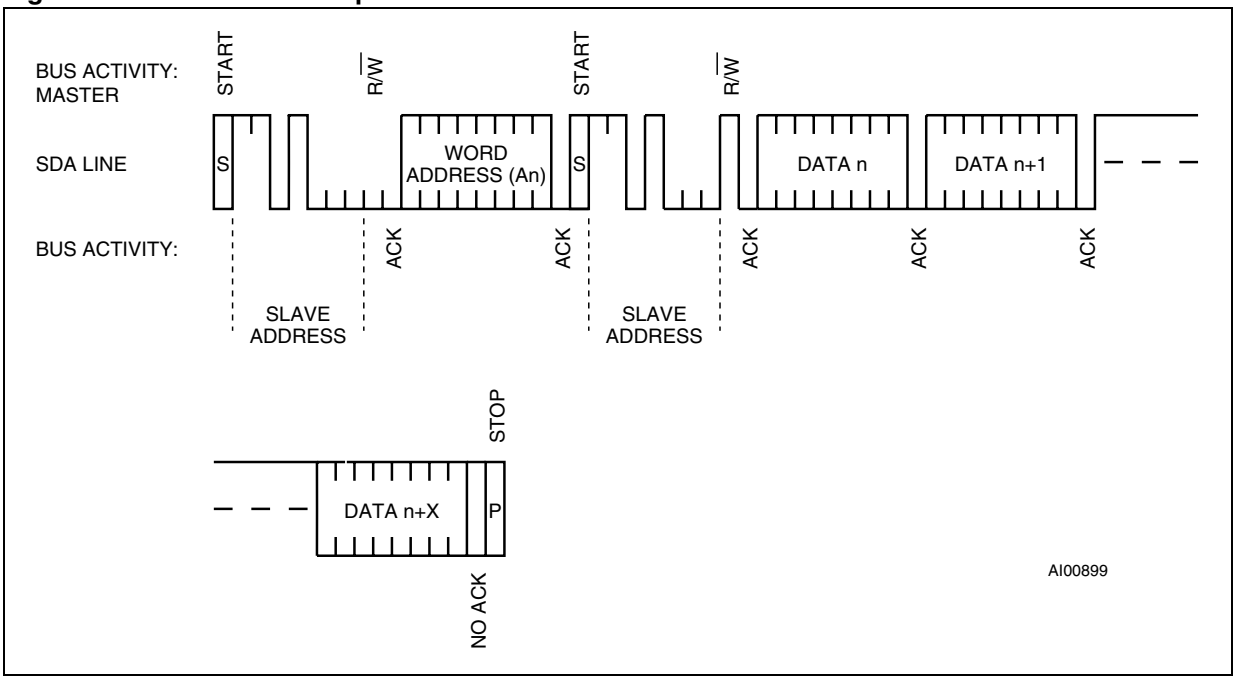
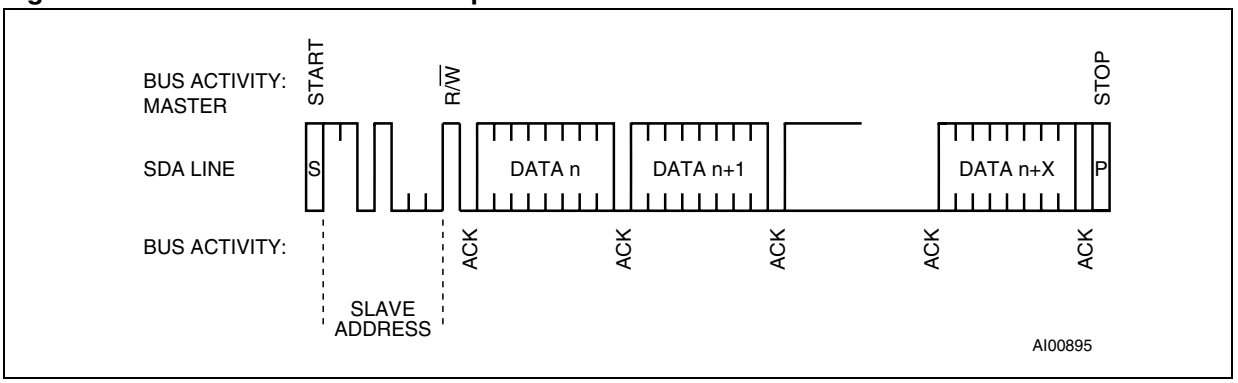


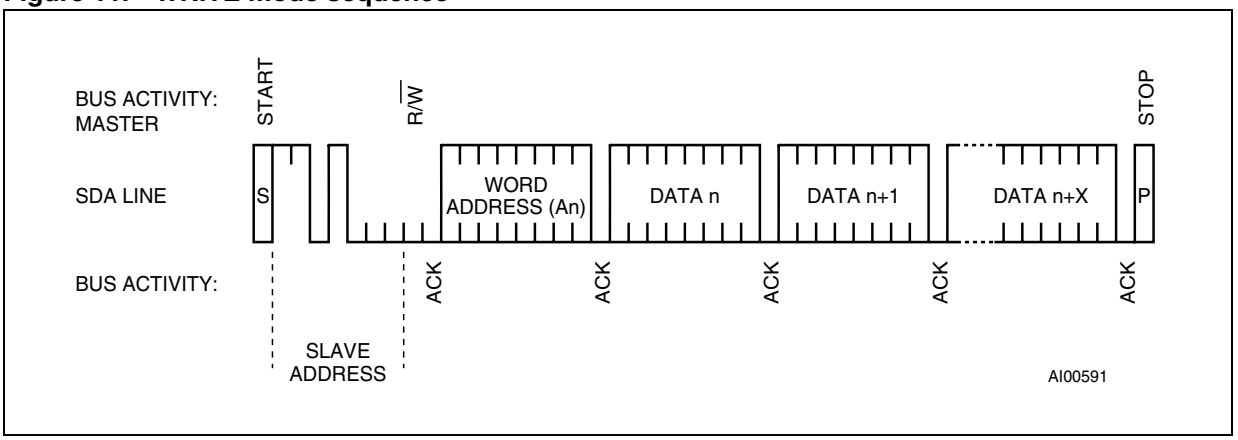
Figure 10. Alternate READ mode sequence



4.4 WRITE mode

In this mode the master transmitter transmits to the M41T00AUD slave receiver. Bus protocol is shown in *Figure 11*. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the device is strobed in next and the internal address pointer is incremented to the next location within the device on the reception of an acknowledge clock. The M41T00AUD slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte (see *Figure 8*).

Figure 11. WRITE mode sequence



4.5 Data retention mode

With valid V_{CC} applied, the M41T00AUD can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41T00AUD will automatically deselect, write protecting itself when V_{CC} falls (see *Figure 13*).

5 M41T00AUD clock operation

5.1 Clock registers

The 10-byte Register Map (see *Table 2*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format.

Seconds, Minutes, and Hours are contained within the first three registers. Bits D6 to D0 or register 00h (seconds register) contain the seconds count in BCD format with values in the range 0 to 59. Bit D7 is the ST or stop bit, described below, and is not affected by the timekeeping operation, but users must avoid inadvertently altering it when writing the seconds register.

Setting the ST bit to a 1 will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain on the backup battery. When reset to a 0 the oscillator restarts within one second.

In order to ensure oscillator start-up after the initial power-up, set the ST bit to a 1 then write it to 0. This sequence enables the "kick start" circuit which aids the oscillator start-up by temporarily increasing the oscillator current. This will guarantee oscillator start-up under worst case conditions of voltage and temperature. This feature can be employed anytime the oscillator is being started but should not occur on subsequent power-ups when the oscillator is already running.

Bits D6 to D0 of register 01h (Minutes Register) contain the minutes count in BCD format with values in the range 0 to 59. Bit D7 always reads 0. Writing it has no effect.

Bits D5 to D0 of register 02h (Century/ Hours Register) contain the hours in BCD format with values in the range 0 to 23. Bits D7 and D6 contain the century enable bit (CEB) and the century bit (CB). CB provides a one-bit indicator for the century. The user can apply his preferred convention for defining the meaning of this bit. For example, 0 can mean the current century, and 1 the next, or the opposite meanings may be used.

When enabled, CB will toggle every 100 years. Setting CEB to a 1 enables CB to toggle at the turn of the century, either from 0 to 1 or from 1 to 0, depending on its initial state, as programmed by the user. When CEB is a 0, CB will not toggle.

Bits D2 through D0 of Register 03h (day register) contain the day of the week in BCD format with values in the range 0 to 7. Bits D3 and D7 will always read 0. Writes to them have no effect. Bits D6, D5 and D4 will power up in an indeterminate state.

Register 04h contains the date (day of month) in BCD format with values in the range 01 to 31. Bits D7 and D6 always read 0. Writes to them have no effect.

Register 05 h is the Month in BCD format with values in the range 1 to 12. Bits D7, D6 and D5 always read 0. Writes to them have no effect.

Register 06h is the years in BCD format with values in the range 0 to 99. Writing to any of the registers 00h to 06h, including the control bits therein, will result in updates to the counters and resetting of the internal clock divider chain including the 256/512Hz tone generator. The updates do not occur immediately after the write(s), but occur upon completion of the current write access. This is described in greater detail in the next section.

Registers 07h and 09h also contain clock control and status information. These registers can be written at any time without affecting the timekeeping function.

Register 08 is the calibration register. Calibration is described in detail in the Clock calibration section. Bit D7 is the OUT bit and controls the discrete output pin $\overline{IRQ}$/FT/OUT as described in *Table 5*.

5.1.1 Halt bit operation

Bit D7 of register 09 h is the HT or halt bit. Whenever the device switches to backup power, it sets the HT bit to 1 and stores the time of power down in the transfer buffer registers. This is known as power-down time stamp. During normal timekeeping, once per second, the transfer buffer registers are updated with the current time. When HT is 1, that updating is halted. The clock continues to keep time but the periodic updates do not occur.

Upon power up, reads of the clock registers will return the time of power down (assuming adequate backup power was maintained while V_{CC} was off). After the user clears the HT bit by writing it to 0, subsequent reads of the clock registers will return the current time.

At power up, the user can read the time of power down, and then clear the HT bit to allow updates. The next read will return the current time. Knowing both the power up time and the power down time allows the user to calculate the duration of power off.

In addition to the HT bit getting set to 1 automatically at power down, the user can also write it to 1 to halt updating of the registers.

5.1.2 Oscillator fail detect operation

Bits D5 and D4 of register 09 h contain the oscillator fail flag (OF) and the oscillator fail interrupt enable bit (OFIE). If the 32 KHz oscillator drops four or more pulses in a row, as might occur during an extended outage while backed up on a capacitor, the OF bit will be set to 1. This provides an indication to the user of the integrity of the timekeeping operation. Whenever the OF bit is a 1, the system should consider the time to be possibly corrupted due to operating at too low a voltage. The OF bit will always be 1 at the initial power up of the device. The OF bit is cleared by writing it to 0. At the initial power up, users should wait three seconds for the oscillator to stabilize before clearing the OF bit.

OFIE can be used to enable the device to assert its interrupt output whenever an oscillator failure is detected. The oscillator fail interrupt will drive the $\overline{IRQ}$/FT/OUT pin as described in Table 5. The interrupt is cleared by writing the OF bit to 0. Setting OFIE enables the oscillator fail interrupt. Clearing it to 0 disables it, but the OF will continue to function regardless of OFIE.

5.1.3 Trickle charger

Bits D6 and D3 to D0, of register 09h, control the trickle charge function. It is described in detail in the Trickle Charge Circuit section.

5.2 Reading and writing the clock registers

The counters used to implement the timing chain in the real-time clock are not directly accessed by the serial interface. Instead, as depicted in *Figure 12*, reads and writes are buffered through a set of transfer registers. This ensures coherency of the timekeeping function.

During writes of the timekeeping registers (00h to 06h), the write data is stored in the buffer transfer registers until all the data is written, then the register contents are simultaneously transferred to the counters thus updating them. The update is triggered either by a STOP condition or by a write to one of the non RTC registers, 07h to 09h. If any of the buffer transfer registers are not written, then the corresponding counters are not updated. Instead, those counters will retain their previous contents when the update occurs.

Similar to the writes, reads access the buffer transfer registers. The device periodically updates the registers with the counter contents. But during reads, the updates are suspended. Timekeeping continues, but the registers are frozen until after a STOP condition or a non RTC register (07h to 09h) is read. Suspending the updates ensures that a clock roll-over does not occur during a user read cycle.

The seven clock registers may be read one byte at a time, or in a sequential block. The calibration, audio and Control2 registers, location 07 h to 09 h, may be accessed independently.

Provision has been made to ensure that a clock update does not occur while any of the seven clock addresses are being read. During a clock register read (addresses 00h to 06h), updates of the clock transfer buffer registers are halted. The clock counters continue to keep time, but the contents of the transfer buffer registers is frozen at the time that the read access began.

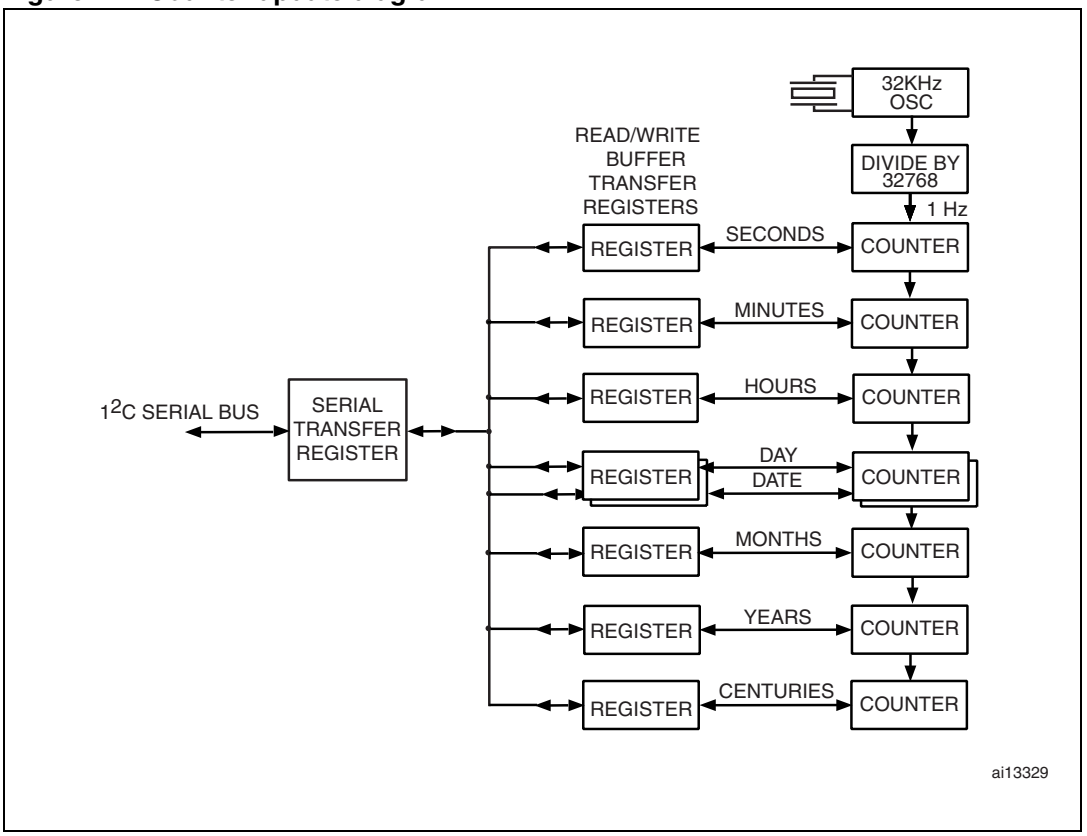
This prevents a transition of data during the READ. For example, without the halt function, if the time incremented past midnight in the middle of an access sequence, the user might begin reading at 11:59:59pm and finish at 12:00:00am. The data read might appear as 12:59:59 because the seconds and minutes were read before midnight while the hours were read after. The device prevents this by halting the updates of the registers until after the read access has occurred.

Table 4. M41T00AUD register map(1)

	Bit								Register name	Range
Addr	D7	D6	D5	D4	D3	D2	D1	D0		
00h	ST	10 seconds			Seconds				Seconds	00-59
01h	0(2)	10 minutes			Minutes				Minutes	00-59
02h	CEB	CB	10 hours		Hours (24 hour format)				Century/hours	0-1/00-23
03h	0	Y(3)	Y	Y	0	Day of week			Day	1-7
04h	0	0	10 date		Date: day of month				Date	01-31
05h	0	0	0	10M	Month				Month	01-12
06h	10 years				Year				Year	00-99
07h	OUT	FT	S	<---------- Calibration ---------->					Cal/control	
08h	256/512	TONE	TCH2	MUTE	<----------GAIN ---------->				Audio	
09h	HT	TCFE	OF	OFIE	TCHE3	TCHE2	TCHE1	TCHE0	Control2	

1. Key:
   S = SIGN bit
   FT = Frequency Test bit'
   ST = STOP bit
   OF = Oscillator Fail Detect Flag
   OFIE = Oscillator Fail Interrupt Enable
   OUT = Logic Output
   TCHE3:TCHEO = Trickle Charge Enable bits
   TCFE = Trickle Charge FET bypass Enable
   HT = Halt bit
   TCH2 = Trickle Charge Enable #2
   TONE = Tone on/off select
   CB = Century bit
   CEB = Century Enable bit
   256/512 = Tone frequency select bit
2. 0 bits always read as 0. Writing them has no effect.
3. Y bits are indeterminate at power-up. These are the factory test mode bits, and must be written to 0.

Figure 12. Counter update diagram



5.3 Priority for $\overline{IRQ}$/FT/OUT pin

Three functions share pin 5 of the M41T00AUD. The oscillator fail interrupt ($\overline{IRQ}$), the calibration frequency test output (FT) and the discrete logic output (OUT) all use this pin.

In normal operation, when operating from V_{CC}, the interrupt function has priority over the frequency test function which in turn has priority over the discrete output function.

In the backup mode, when operating from V_{BACK}, the priorities are different. The interrupt and frequency test functions are disabled, and only the discrete output function can be used.

When operating from V_{CC}, if the oscillator fail interrupt enable bit is set (OFIE, D4 of register 09h), the pin is an interrupt output which will be asserted anytime the OF bit (D5 of register 09h) goes true. (See *Section 5* for more details.)

During calibration, the pin can be used as a frequency test output. When FT is a 1 (and OFIE a 0), the device will output a 512Hz test signal on this pin. Users can measure this with a frequency counter and use that result to determine the appropriate calibration register value.

Otherwise, when OFIE is a 0 and FT is a 0, it becomes the discrete logic OUT pin and reflects the value of the OUT bit (D7 of register 07h).

When operating from V_{BACK}, the discrete output function can still be used. The $\overline{IRQ}$/FT/OUT pin will reflect the contents of the out bit.

Note: The $\overline{IRQ}$/FT/OUT pin is open drain and requires an external pull-up resistor.

Table 5. Priority for $\overline{IRQ}$/FT/OUT pin

State	Register bits			$\overline{IRQ}$/FT/OUT pin
	OFIE	FT	OUT	
On V_{CC}	1	X	X	$\overline{OF}$
	0	1	X	512 Hertz
	0	0	1	1
	0	0	0	0
On V_{BACK}	X	X	1	1
	X	X	0	0

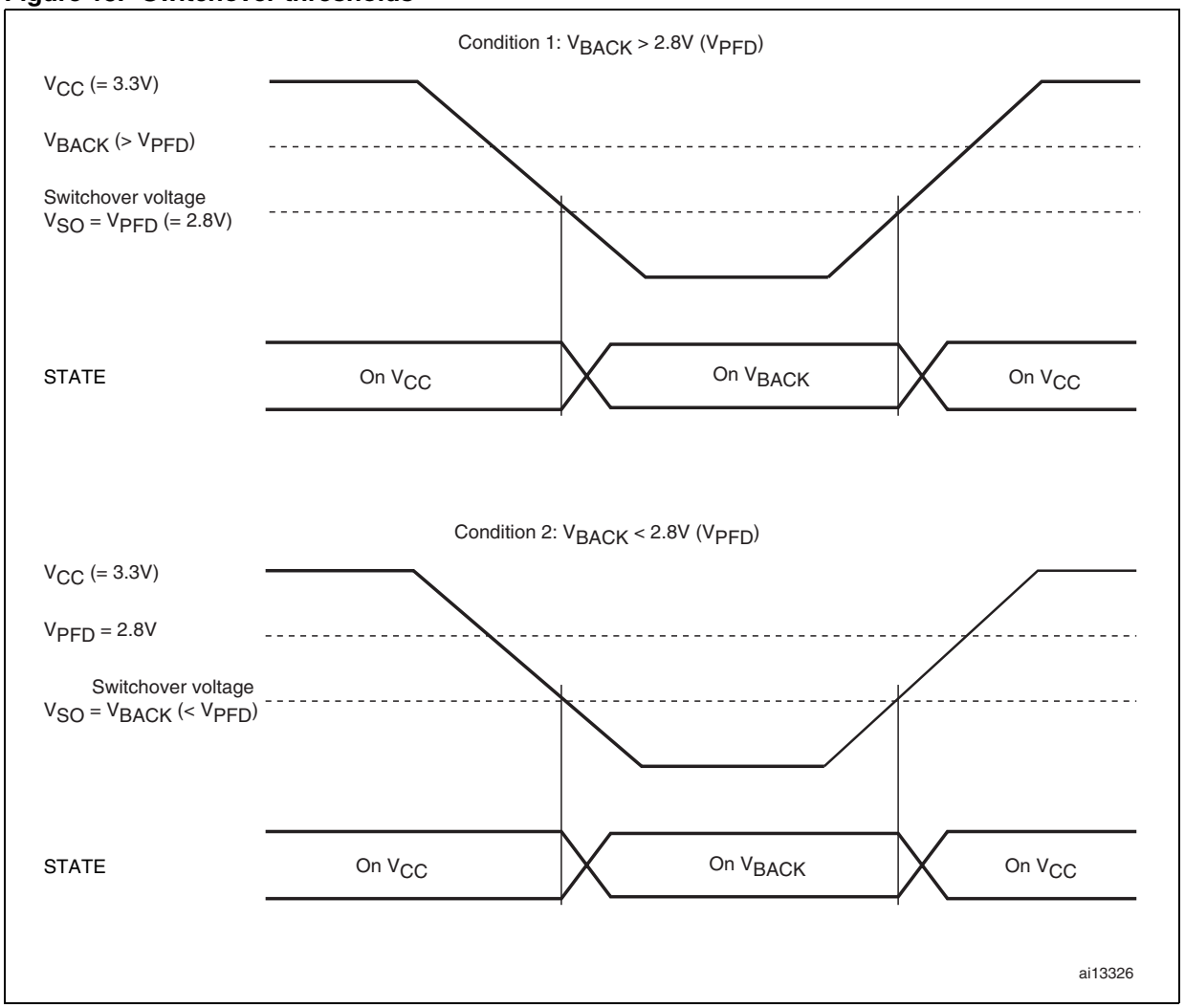
5.4 Switchover thresholds

While the M41T00AUD includes a precision reference for the backup switchover threshold, it is not a fixed value, but depends on the backup voltage, V_{BACK}. The device will always switchover at the lesser of the reference voltage (V_{PFD}, approximately 2.8V) and V_{BACK}. This ensures that it stays on V_{CC} as long as possible before switching to the backup supply.

As shown in *Figure 13*, whenever V_{BACK} is greater than V_{PFD}, switchover occurs when V_{CC} drops below V_{PFD}.

Conversely, when V_{BACK} is less than V_{PFD}, switchover occurs when V_{CC} drops below V_{BACK}. *Table 14* provides the values of these voltages.

Figure 13. Switchover thresholds



5.5 Trickle charge circuit

The M41T00AUD includes a trickle charge circuit to be used with a backup capacitor. It is illustrated in *Table 14*. V_{BACK} is a bi-directional pin. Its primary function is as the backup supply input. (The input nature is not depicted in the figure.) The trickle charge output function is a secondary capability, and reduces the need for external components.

To enable trickle charging, two switches must be closed. A diode is present to prevent current from flowing backwards from V_{BACK} to V_{CC}. A current limiting resistor is also in the path.

An additional switch allows the diode to be bypassed through a 20k resistor. This should charge the capacitor to a higher level thus extending backup life. This switch automatically opens when the device switches to backup thus preventing capacitor discharge to V_{CC}.

Furthermore, at switchover to backup, the other switches open as well. The application must close them after power up to re-enable the trickle charge function.

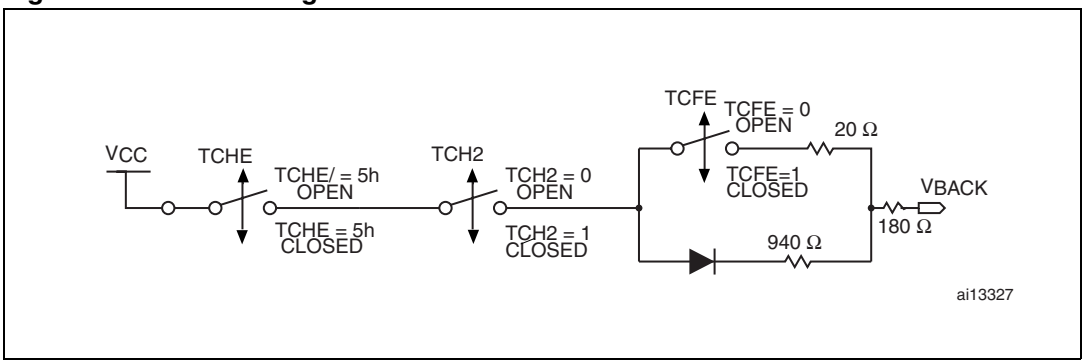
The use of two switches in the chain is to protect against accidental, unwanted charging as might be the case when using battery backup. Additionally, one of the two switches requires four bits to be changed from the default value before it will close. This prevents single bit errors from closing the switch. The four bits, TCHE3:TCHE0, reside in register 09h at bits D3 to D0.

The control bit for the second switch, TCH2, resides in register 08h at bit D5. With this bit in a separate register, two bytes must be written before charging will occur, again protecting against inadvertent charging due to errors.

The control bit for the bypass switch, TCFE, resides in register 09h at bit D6.

To enable trickle charging, the user must set TCHE3:TCHE0 to 5h, and TCH2 to 1. To bypass the diode, TCFE must be set to 1. All three fields must be enabled after each power up.

Figure 14. Trickle charge circuit



6 Clock calibration

The M41T00AUD oscillator is designed for use with a 12.5pF crystal load capacitance. With a nominal ±20 ppm crystal, the M41T00AUD will be accurate to ±35 ppm. When the calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The M41T00AUD design provides the following method for clock error correction.

6.1 Digital calibration (periodic counter correction)

This method employs the use of periodic counter correction by adjusting the number of cycles of the internal 512Hz signal counted in a second. By adding an extra cycle, for 513, a long second is counted for slowing the clock. By reducing it to 511 cycles, a short second is counted for speeding up the clock.

Not every second is affected. The calibration value (bits D4-D0 of register 07h) and its sign bit (D5 of same register) control how often a short or long second is generated.

The basic nature of a 32KHz crystal is to slow down at temperatures above and below 25°C. Whether the temperature is above or below 25°C, the device will tend to run slow. Therefore, most corrections will need to speed the clock up. Hence, the M41T00AUD calibration circuit uses a non-symmetric calibration scheme. Positive values, for speeding the clock up, have more effect than negative values, for slowing it down. A positive value will speed the clock up by approximately 4ppm per step. A negative value will slow it by approximately 2ppm per step.

In the M41T00AUD's calibration circuit, positive correction is applied every 8^{th} minute whereas negative correction is applied every 16^{th} minute. Because positive correction is applied twice as often, it has twice the effect for a given calibration number, N. When the calibration sign bit is positive, N seconds of every 8^{th} minute will be shortened to 511 cycles of the 512Hz clock. When the calibration sign bit is negative, N seconds of every 16^{th} minute will be lengthened to 513 cycles of the 512Hz clock.

When N is positive, one minute will have N seconds which are 511 cycles and the remaining seconds will be 512 cycles. The next seven minutes are nominal with all seconds 512 cycles each.

Example 1:

Sign is 1 and N is 2 (00010b)

The 8-minute interval will be:

2 * 511 + (60-2) * 512 + 7 * 60 * 512 = 245758 cycles long out of a possible

512 * 60 * 8 = 245760 cycles of the 512Hz clock in an 8-minute span.

This gives a net correction of (245760-245758) / 245760 = -8.138ppm

When N is negative, one minute will have N seconds which are 513 cycles and the remaining seconds will be 512 cycles. The next 15 minutes are nominal with all seconds 512 cycles each

Example 2:

Sign is 0 and N is 3 (00010b). The 16-minute interval will be:

3 * 513 + (60-3) * 512 + 15 * 60 * 512 = 491523 cycles long out of a possible

512 * 60 * 16 = 491520 cycles of the 512Hz clock in an 16-minute span.

This gives a net correction of (491520-491523) / 491520 = +6.104ppm

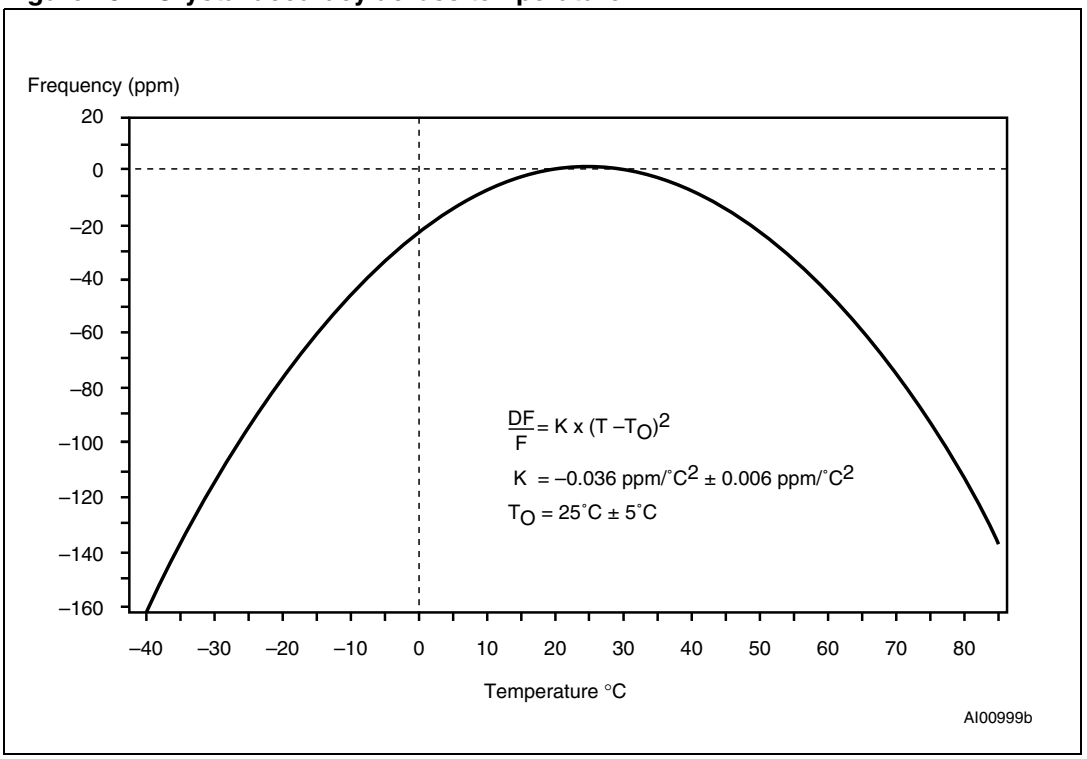
Therefore, each calibration step has an effect on clock accuracy of either -4.068 or +2.034 ppm. Assuming that the oscillator is running at exactly 32,768Hz, each of the 31 steps in the calibration byte would represent subtracting 10.7 or adding 5.35 seconds per month, which corresponds to a total range of -5.5 or +2.75 minutes per month.

Note: The modified pulses are not observable on the frequency test (FT) output, nor will the effect of the calibration be measurable real-time, due to the periodic nature of the error compensation.

Table 6. Digital calibration values

Calibration value DC4-DC0		Calibration result, in ppm, rounded to the nearest integer	
Decimal	Binary	Slowing sign DCS = 0	Speeding sign DCS = 1
0	00000	+ 0 ppm	– 0 ppm
1	00001	+ 2 ppm	– 4 ppm
2	00010	+ 4 ppm	– 8 ppm
3	00011	+ 6 ppm	– 12 ppm
4	00100	+ 8 ppm	– 16 ppm
5	00101	+ 10 ppm	– 20 ppm
6	00110	+ 12 ppm	– 24 ppm
7	00111	+ 14 ppm	– 28 ppm
8	01000	+ 16 ppm	– 33 ppm
9	01001	+ 18 ppm	– 37 ppm
10	01010	+ 20 ppm	– 41 ppm
11	01011	+ 22 ppm	– 45 ppm
12	01100	+ 24 ppm	– 49 ppm
13	01101	+ 26 ppm	– 53 ppm
14	01110	+ 28 ppm	– 57 ppm
15	01111	+ 31 ppm	– 61 ppm
16	10000	+ 33 ppm	– 65 ppm
17	10001	+ 35 ppm	– 69 ppm
18	10010	+ 37 ppm	– 73 ppm
19	10011	+ 39 ppm	– 77 ppm
20	10100	+ 41 ppm	– 81 ppm
21	10101	+ 43 ppm	– 85 ppm
22	10110	+ 45 ppm	– 90 ppm
23	10111	+ 47 ppm	– 94 ppm
24	11000	+ 49 ppm	– 98 ppm
25	11001	+ 51 ppm	– 102 ppm
26	11010	+ 53 ppm	– 106 ppm
27	11011	+ 55 ppm	– 110 ppm
28	11100	+ 57 ppm	– 114 ppm
29	11101	+ 59 ppm	– 118 ppm
30	11110	+ 61 ppm	– 122 ppm
31	11111	+ 63 ppm	– 126 ppm
N		+N/491520 (per minute)	–N/245760 (per minute)

Figure 15. Crystal accuracy across temperature



7 Audio section operation

The audio section is comprised of five main parts. The input includes a summing amplifier. A minimum 10kΩ feedback resistor is required. With that and 20kΩ input resistors, the input signals will be summed at unity gain.

An audio switch follows the amplifier. A tone, selectable between 256 and 512 Hz, can be inserted into the audio stream in lieu of the input amplifier's output.

A low pass filter is next with a cut off of 8 kHz. To get a band pass with a 100 Hz low end, the user should place an appropriate coupling capacitor at the input pin.

Figure 16. Audio section diagram

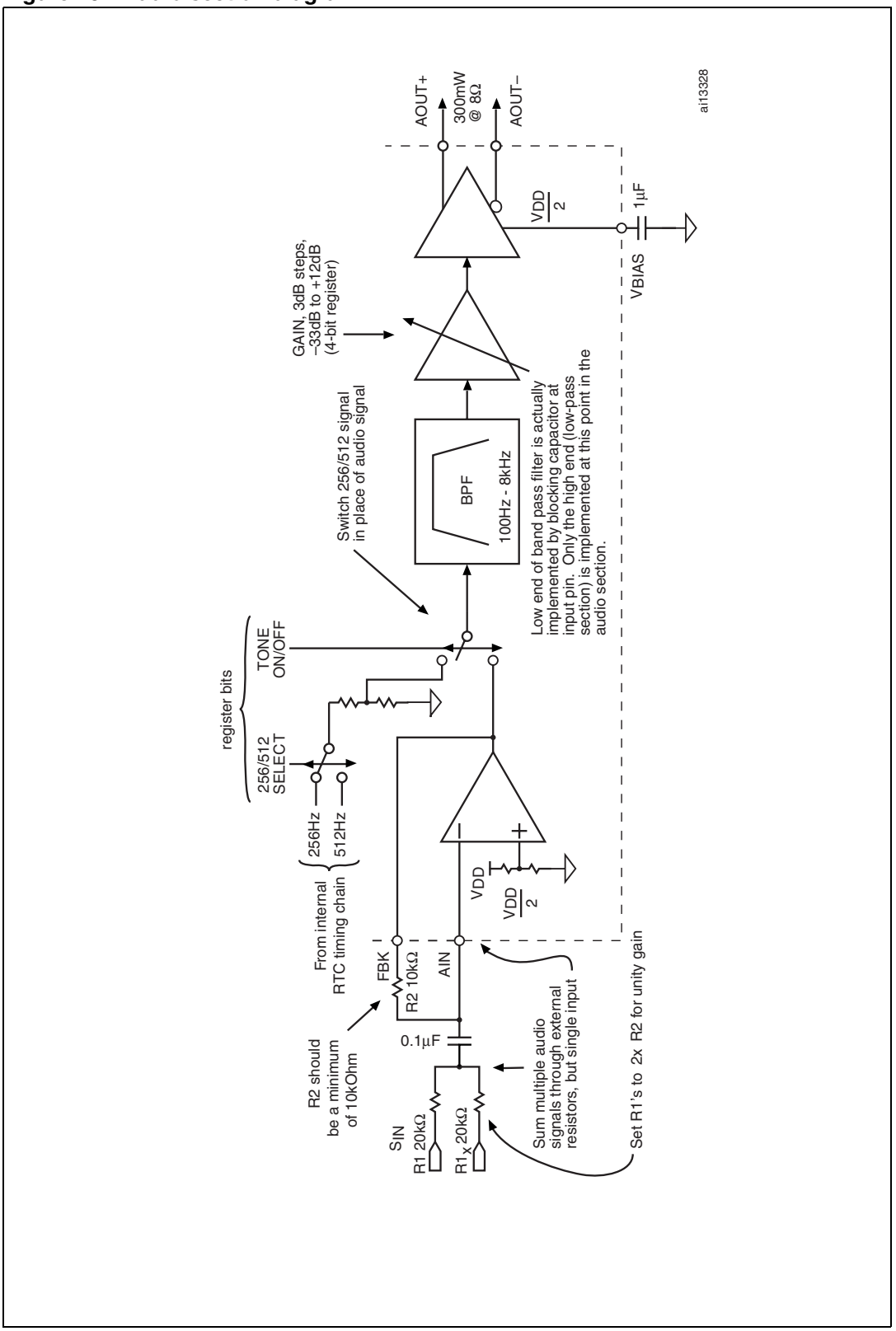


Table 7. MUTE and GAIN(1) values (V_{CC} = 3.3V and ambient temperature = 25°C)

MUTE	GAIN		Audio gain (dB)			A_V. scalar gain
	Binary	Hex	Min	Typ	Max	Typ
1	XXXX	X	Off			Off
0	1111	F	+12			4
0	1110	E	+7	+9	+11	2.8
0	1101	D	+6			2
0	1100	C	+3			1.4
0	1011	B	-1	0	+1	1
0	1010	A	-3			0.708
0	1001	9	-6			0.5
0	1000	8	-9			0.355
0	0111	7	-12			0.251
0	0110	6	-15			0.178
0	0101	5	-20	-18	-16	0.126
0	0100	4	-23	-21	-19	0.089
0	0011	3	-24			0.063
0	0010	2	-27			0.045
0	0001	1	-30			0.032
0	0000	0	-33			0.022

1. Target specification. Further testing will determine final min/max limits for GAIN values of E, B, 5 and 4.

7.1 Gain

The programmable gain stage follows the band pass filter. It provides between –33 and +12dB of gain, in 3dB steps (+/-1dB per step). The gain is selected by the GAIN bits, D3-D0 of register 08h, as listed in *Table 4*. A MUTE bit, D4 of the same register, allows the audio to be cut off altogether.

At the first power up, GAIN will be initialized to its lowest value, 0, corresponding to a gain of –33dB. Furthermore, MUTE will be set thus cutting off all audio.

On subsequent power ups, GAIN is unaffected, but the MUTE bit is always set to turn off the audio at power up.

The final section is the output driver. It has a differential output capable of driving 300mW into an 8Ω load.

The overall gain of the M41T00AUD is defined as the ratio of the AC output voltage, A_{OUT}, and the AC input voltage, S_{IN}, as shown in *Figure 16*. The 0.1uF input coupling capacitor blocks any DC in the input signal.

Equation 1

$$\text{Overall gain} = A_{OUT} / S_{IN}$$

A_{OUT} is measured between the output pins $AOUT^+$ and $AOUT^-$.

$$A_{OUT} = AOUT^+ - AOUT^-$$

Each of the output levels is determined by the ratio of the feedback and input resistors along with the GAIN value.

$$AOUT^+ = S_{IN} \times A_V \times R2/R1$$

$$AOUT^- = -S_{IN} \times A_V \times R2/R1$$

where A_V is the scalar gain as shown in *Table 7*. Substituting these into Equation 1 above yields:

$$A_{OUT} = S_{IN} \times A_V \times R2/R1 - (-S_{IN} \times A_V \times R2/R1) = 2\ S_{IN} \times A_V \times R2/R1$$

With R1 = 2*R2, this reduces to $A_{OUT} = S_{IN} \times A_V$. Thus, when R1 = 2*R2, the gain levels in *Table 7* reflect overall gain of the circuit (at mid-band frequencies, about 1kHz with the indicated 0.1uF capacitor). For GAIN set to B (0dB, $A_V = 1$), the output voltage will be equal to the input (±1dB).

7.1.1 Gain tolerance

Two tolerance parameters apply to the gain levels. As shown in *Table 7*, upper and lower limits are listed for four of the GAIN values (4, 5, Bh and Eh). For GAIN=Bh, the tolerance is ±1dB. This means the end-to-end gain of the part, with R1 = 2*R2, will be 0±1dB. For GAIN=4, 5 and Eh, the tolerance is ±2dB. At each of these three settings, as shown in table 7, the gain will be within 2dB of the listed typical value. For GAIN =E, the end-to-end gain will be between +7 and +11 dB (9±2dB).

The other parameter pertains to the gain step size, a relative measurement. It is shown in *Table 16* as 3±1dB. For any gain setting in *Table 7*, the next higher (or lower) setting is guaranteed to be between 2 and 4 dB higher (or lower). For example, even though no upper and lower limits are shown for GAIN = Ch, it is tested to be at 3±1dB of the case when GAIN=Bh, one step below. If GAIN=Bh tests to -0.5dB, then GAIN=Ch is tested to have an end-to-end gain of 2.5±1dB. If GAIN=Bh tests to +0.5dB, then GAIN=Ch is tested to be 3.5±1dB.

This applies to all steps except the lowest one (from GAIN=0 to GAIN=1) which is not tested.

In summary, for GAIN=1 to GAIN=Fh, all steps are tested to have a 1dB step size tolerance of the listed 3dB step size. The unity gain setting, Bh, will have an end-to-end gain of 0±1dB while the three levels for GAIN=4, 5 and Eh are tested to be within ±2dB of the typical gain values listed in *Table 7*.

7.2 Wake-up time: T_{WU}

When the device powers on, the bypass capacitor C_{BIAS} will not be charged immediately. As C_{BIAS} is directly linked to the bias of the amplifier, the amplifier will not work properly until the capacitor is charged. The time to reach this voltage is called the wake-up time or T_{WU} and is specified in the electrical characteristics, table 15, for C_{BIAS} = 1µF.

8 Initial conditions

The first time the M41T00AUD is powered up, some of its registers will automatically have their bits set to pre-determined levels as depicted in the *Table 5*. Typically, these values are set to benign levels to ensure predictable operation of the device.

ST, the stop bit, is a 0 at first power up thus enabling the oscillator to run without need of user intervention. On subsequent power ups, it is not altered by the device and remains at the last value programmed by the user. All other bits listed as unchanged (UC) in the table behave similarly during power cycles.

The HT or halt bit is always set to 1 thus halting updates of the transfer buffer registers. The user must write it to 0 to allow updates to resume.

The discrete output function available on the $\overline{IRQ}$/FT/OUT pin is set to 1. This is an open drain output, and thus a 1 represents a high impedance condition.

FT or frequency test is always disabled on power ups. The OF or oscillator fail bit will always be 1 on the first power up since the oscillator is always off prior to the first application of V_{CC}.

The trickle charger is always turned completely off after any power up. The bits affecting it are set to levels which keep all the trickle charge switches open. Both TCH2 and TCFE are 0 which opens their corresponding switches. TCHE3:TCHE0 are set to Ah, which is the exact opposite of the value (5) required to close the corresponding switch.

On first power up, the tone selects bits, /256/512 and TONE, are set to select the 512 hertz tone, but have the function disabled (see *Section 7*). On subsequent power ups, the /256/512 select bit remains unchanged, but TONE is always cleared. Furthermore, the MUTE bit is always set to MUTE on all power ups, disabling all audio.

The four-bit audio gain value is always set to the lowest setting (0) on initial power up, but remains unaffected by subsequent power cycles.

The 5-bit calibration register and its associated sign bit are set to 0 on initial power up thus resulting in no correction applied to the timekeeping operation. On subsequent power ups, the contents are not altered.

Table 8. Initial values

Condition	ST	HT	OUT	FT	OF	OFIE	TCHE 3:0	TCH2	TCFE	/256/ 512	TONE	MUTE	GAIN	Cali-bration
Initial power-up(1)	0 On	1	1	0	1	0 Off	Ah Off	0 Off	0 Off	1 512	0 Off	1 MUTE	0 -33dB	0
Subsequent power-up (with battery back-up)	UC(2)	1	UC	0	UC	UC	Ah Off	0 Off	0 Off	UC	0 Off	1 MUTE	UC	UC

1. State of other control bits undefined
2. UC = unchanged

9 Maximum ratings

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents

Table 9. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–55 to 150	°C
T_J	Maximum junction temperature	150	°C
R_{THJA}	Thermal resistance junction to ambient	200	°C/W
V_{CC}	Supply voltage	–0.3 to 4.5	V
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to Vcc+0.3	V
I_{OA}	Audio output current	300	mA
I_{OD}	Digital output current	20	mA
P_D	Power dissipation	Internally limited	

1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

Caution: Negative undershoots below -0.3V are not allowed on any pin while in the back-up mode.

10 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 10. Operating and AC measurement conditions(1)

Parameter	M41T00AUD
Supply voltage (V_{CC})	3.0 to 3.6V
Ambient operating temperature (T_A)	0 to 70°C
Digital load capacitance (C_L)	100pF
Audio load resistance (R_L)	≥ 8Ω
Digital input Rise and Fall times	≤ 5ns
Digital input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Digital input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$

1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 17. AC testing Input/Output waveform

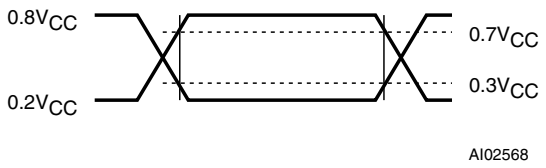


Table 11. Input/output characteristics (25°C, f = 1MHz)

Symbol	Parameter (1)	Min	Max	Unit
C_{IND}	Input capacitance, digital inputs		7	pF
C_{OUTD}(2)	Output capacitance, digital outputs		10	pF
t_{LP}	I^2C low-pass filter input time constant (SDA and SCL)		50	ns

1. Effective capacitance measured with power supply at 3.3V; sampled only, not 100% tested
2. Outputs deselected

Table 12. DC characteristics

Symbol	Parameter	Test condition(1)	Min	Typ	Max	Unit
I_{LI}	Input leakage current	$0V \leq V_{IN} \leq V_{CC}$, SCL pin			±1	µA
I_{LO}	Output leakage current	$0V \leq V_{OUT} \leq V_{CC}$, OUT and SDA pins			±1	µA
I_{CC1}	Active supply current	No audio (AIN = V_{BIAS}), I^2C bus active at 400kHz		6.6	14.7	mA
I_{CC2}	Standby supply current	No audio (AIN = V_{BIAS}), I^2C bus not active, SCL = 0Hz All inputs ≥ V_{CC} – 0.2V or ≤ V_{SS} + 0.2V		6.4	14.3	mA
V_{IL}	Input Low voltage		–0.3		$0.3V_{CC}$	V
V_{IH}	Input High voltage		$0.7V_{CC}$		V_{CC} + 0.3	V
V_{OL}	Output Low voltage	I_{OL} = 3.0mA			0.4	V
	Output Low Voltage (open drain)(2)	I_{OL} = 3.0mA			0.4	V
	Pull-up supply voltage (open drain)	$\overline{IRQ}$/FT/OUT, SDA, SCL			Vcc	V
V_{BACK}(3)	RTC back-up supply voltage		1.7		V_{CC}	V
I_{BACK}	RTC backup supply current	T_A = 25°C, V_{CC} = 0V oscillator ON, V_{BACK} = 3V		0.6	1	µA

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where otherwise noted).
2. For open drain pins $\overline{IRQ}$/FT/OUT and SDA
3. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) when a battery is used.

Table 13. Crystal electrical characteristics

Symbol	Parameter (1)(2)	Min	Typ	Max	Units
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			40	KΩ
C_L	Load capacitance		12.5		pF

1. Externally supplied if using the SO8 package. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at http://xxx.kds.info/index_en.htm for further information on this crystal type.
2. Load capacitors are integrated within the M41T00AUD. Circuit board layout considerations for the 32.768kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

Figure 18. Power down/up mode AC waveforms

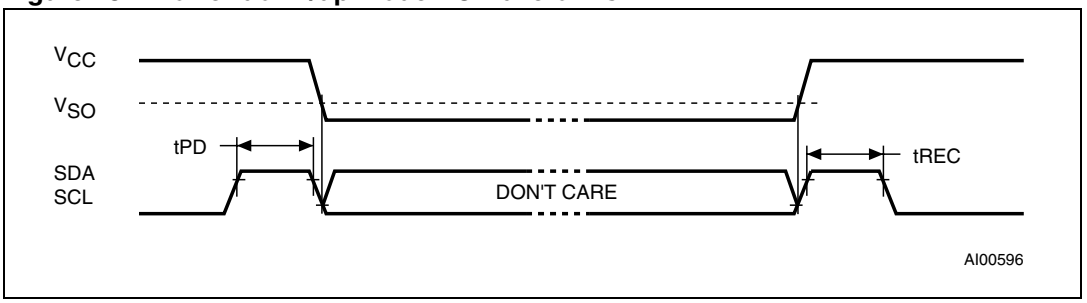


Table 14. RTC power down/up AC characteristics

Symbol	Parameter(1)(2)	Min	Typ	Max	Unit
t_{PD}	SCL and SDA at VIH before power down	0			ns
t_{rec}	SCL and SDA at VIH after power up	10			µs

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where otherwise noted).
2. V_{CC} fall time should not exceed 5mV/µs.

Table 15. RTC power down/up trip points DC characteristics

Symbol	Parameter(1)(2)		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect		2.60	2.8	2.95	V
	Hysteresis			10		mV
V_{SO}	Back-up switchover voltage (V_{CC} < V_{BACK}; V_{CC} < V_{PFD})	2.0 < V_{BACK} < V_{PFD}		V_{BACK}		V
		V_{BACK} > V_{PFD}		V_{PFD}		V
	Hysteresis			10		mV

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where otherwise noted).

Table 16. Audio section electrical characteristics, valid for V_{CC} = 3.3V and T_{AMB} = 25°C (except where otherwise noted)(1)

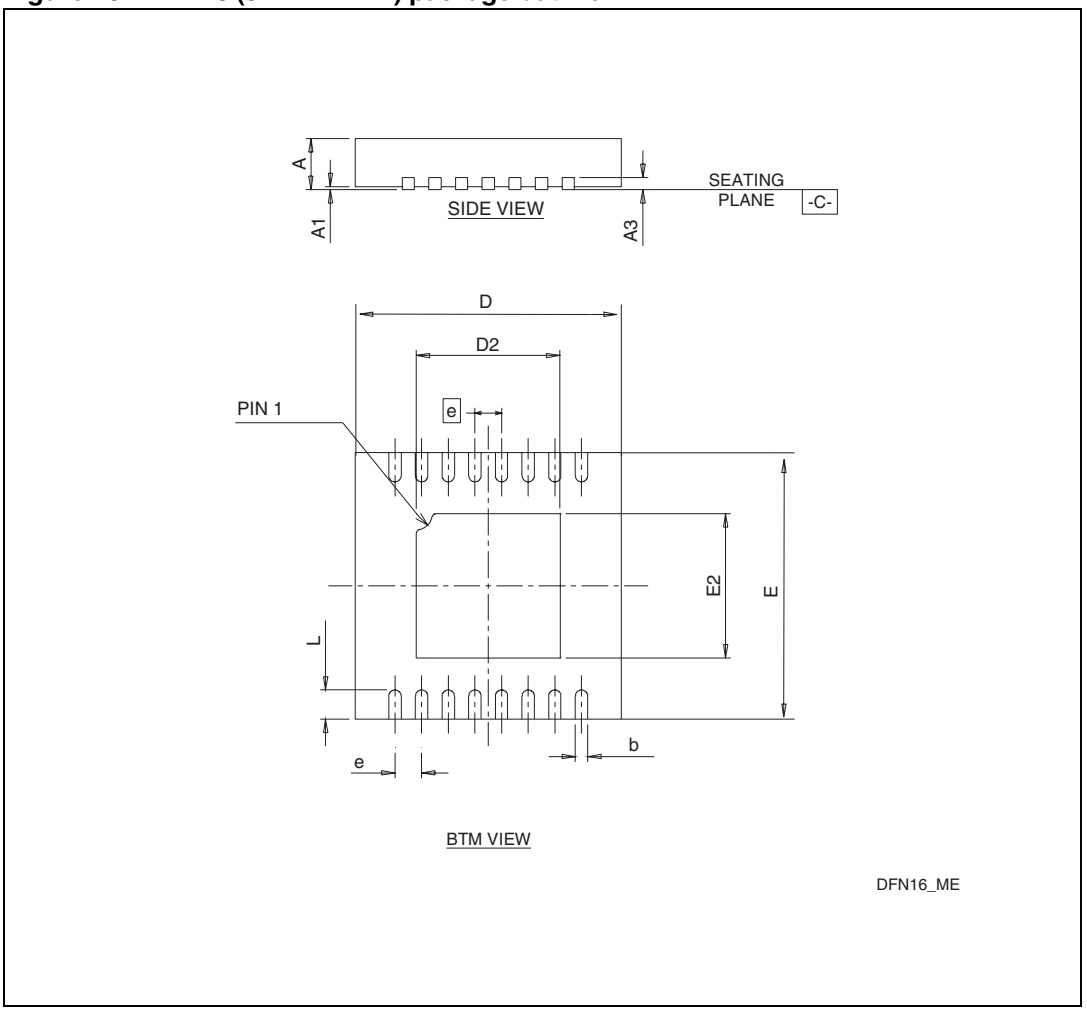
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OO}	Output offset voltage	No input signal, RL = 8Ω		10	100	mV
$P_{O\text{-}MAX}$	Maximum output power	THD = 2% Max, f = 1kHz, RL = 8Ω	300	375		mW
P_{SRR}	Power supply rejection ratio	RL = 8Ω, Av = 2, V_{RIPPLE} = 200mV_{PP} audio input grounded f = 217Hz	55	61		dB
	Gain step size	GAIN steps 1-2 to E-F (1)	2	3	4	dB
TWU	Wake-up time after power up	C_{BIAS} = 1µF			150	ms

1. The lowest step, from GAIN = 0 to GAIN = 1, is not tested.

11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 19. DFN16 (5mm x 4mm) package outline



1. Drawing is not to scale.

Table 17. DFN16 (5mm x 4mm) package mechanical data

Sym	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.02	0.05	0.00	0.0007	0.002
A3		0.20			0.008	
b	0.20	0.25	0.30	0.008	0.010	0.012
D		5.00			0.197	
E		4.00			0.157	
D2	4.20	4.35	4.45	0.165	0.171	0.175
E2	2.30	2.45	2.55	0.091	0.096	0.100
e		0.50			0.020	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20			0.008		

12 Part numbering

Table 18. Ordering information scheme

Example: M41T00AUD D 1 F

Device type

M41T00AUD

Package

D = Lead-free 5mm x 4mm DFN

Temperature range

1 = 0°C to 70°C

Shipping method

E = ECOPACK® lead-free ICs in tube

F = ECOPACK® lead-free ICs in tape & reel

13 Revision history

Table 19. Document revision history

Date	Revision	Changes
01-May-2007	1	Initial release.
13-Dec-2007	2	Minor text changes; updated footnote 1 in *Table 13*.

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